WHAT IS CLAIMED IS:

1. An ATM header conversion circuit comprising:

entry data storage means for storing, as entry data, first and second ATM header data paired at each of a plurality of addresses;

partial collation means for partially collating inputted header data with one of said first and second ATM header data stored in said entry data storage means for each address on the basis of a designation signal representative of a collation position of said ATM header data being converted, and for outputting a collation result for each address;

address extraction means for extracting, on the basis of the collation result for each address, an address in said entry data storage means at which the collation result shows coincidence; and

header outputting means for outputting, as converted ATM header data, the other of said first and second ATM header data at said address extracted by said address extraction means, from said entry data storage means.

2. The ATM header conversion circuit according to claim 1, wherein said designation signal representative of the collation position of one of said first and second ATM header data is generated in units of bits, and said partial collation means collates said inputted header data with one of said first and second ATM header data in units of bits.

3. The ATM header conversion circuit according to claim 1, wherein said designation signal representative of the collation position of one of said first and second ATM header data is generated in unit of word, and said partial collation means collates the

inputted header data with one of said first and second ATM header data in unit of word.

4. The ATM header conversion circuit according to claim 1, further comprising entry data partial-readout means for partially reading out, in the form of one word, one of said first or second ATM header data stored in said entry data storage means on the basis of a designation signal generated in the form of word and a specified readout address in said entry data storage means.

5. The ATM header conversion circuit according to claim 1, further comprising entry data partial-write means for partially writing, in the form of one word, one of first and second ATM header data in said entry data storage means on the basis of a designation signal generated in unit of word and a write address in said entry data storage means.

6. The ATM header conversion circuit according to claim 3, wherein the number of words each to be used for said designation signal is made variable.

7. The ATM header conversion circuit according to claim 3, wherein the number of bits to be allocated to one word is made variable.

8. The ATM header conversion circuit according to claim 3, wherein the number of words each to be used for the designation signal and the number of bits to be allocated to one word are made variable.

9. The ATM header conversion circuit according to claim 1, wherein said header outputting means is made to output, in addition to said converted ATM header data, a corresponding address in said entry data storage means.

10. An ATM header conversion circuit comprising:

entry data storage means for storing ATM header data, which remain unchanged before and after conversion, as entry data in a state associated with first and second addresses paired;

full collation means for fully collating inputted header data with said ATM header data, stored in said entry data storage means, at each of said pairs of first and second addresses to output a collation result at each of said pairs of first and second addresses;

address extraction means for extracting, on the basis of said collation result at each of said pairs of first and second addresses, said first and second addresses in said entry data storage means at which said collation result shows coincidence;

converted ATM header storage means for previously storing said ATM header data after conversion in a state associated with said first and second addresses in said entry data storage means; and

readout means for selecting one of said first and second addresses extracted in said address extraction means on the basis of a direction of the ATM header conversion to read out said ATM header data at the selected address from said converted ATM header storage means.

11. The ATM header conversion circuit according to claim 10, wherein said ATM header conversion direction is designated according to a network through which header data is inputted to said full collation means.

12. The ATM header conversion circuit according to claim 1, further comprising a connection whose one side has a plurality of divided ports so that addresses in said entry data storage means correspond to the numbers of said ports, respectively.

13. The ATM header conversion circuit according to claim 10, further comprising a connection whose one side has a plurality of divided ports so that addresses in said entry data storage means correspond to the numbers of said ports, respectively.

14. The ATM header conversion circuit according to claim 1, further comprising a connection whose one side has a plurality of divided ports, and addresses in said entry data storage means include the numbers of said ports, respectively.

15. The ATM header conversion circuit according to claim 10, further comprising a connection whose one side has a plurality of divided ports, and addresses in said entry data storage means include the numbers of said ports, respectively.

16. The ATM header conversion circuit according to claim 14, wherein header data inputted through one non-divided side of said connection is collated on the basis of said designation signal representative of the collation position of said ATM header data

being converted, and said ATM header data converted is outputted to one of said plurality of divided ports of the other side of said connection on the basis of said port number included in said address.

17. The ATM header conversion circuit according to claim 14, wherein said port numbers are added to said ATM header data on the divided side of said connection and stored in said entry data storage means, and said ATM header data and said port numbers are partially collated on the basis of said designation signal representative of the collation position of said ATM header data being converted.

18. The ATM header conversion circuit according to claim 14, wherein said port numbers are added to said ATM header data on the divided side of said connection and stored in said entry data storage means while said ATM header data on the non-divided side of said connection is stored intact, and in a case in which said ATM header data is inputted through the divided side of said connection, said ATM header data, together with said port number, is partially collated on the basis of said designation signal representative of the collation position of said ATM header data being converted, while in a case in which said ATM header data is inputted through the non-divided side of said connection, only said ATM header data undergoes partial collation.

19. The ATM header conversion circuit according to claim 1, wherein connection information is added to said entry data and stored in said entry data storage means.

20. The ATM header conversion circuit according to claim 19, wherein said connection information, together with the converted header data corresponding to said inputted header data, is outputted on the basis of said designation signal representative of the collation position of said ATM header data being converted.

21. The ATM header conversion circuit according to claim 1, wherein, of said ATM header data stored in said entry data storage means, a VPI/VCI inhibited as input in a system is set as an initial value.

22. The ATM header conversion circuit according to claim 10, wherein, of said ATM header data stored in said entry data storage means, a VPI/VCI inhibited as input in a system is set as an initial value.

23. The ATM header conversion circuit according to claim 1, wherein, of said ATM header data stored in said entry data storage means, a VPI/VCI which is not required to be registered is set as an initial value.

24. The ATM header conversion circuit according to claim 10, wherein, of said ATM header data stored in said entry data storage means, a VPI/VCI which is not required to be registered is set as an initial value.

25. The ATM header conversion circuit according to claim 1, further comprising:

first multiple-coincidence counting means placed in an odd-number position for counting the coincidences with a plurality of entry data on the basis of a collation result on each entry data stored in said entry data storage means and the last multiple-coincidence information on said entry data and further for communicating a count result to the next multiple-coincidence counting means; and

second multiple-coincidence counting means placed in an even-number position for detecting the coincidences with a plurality of entry data on the basis of a collation result on each entry data stored in said entry data storage means, the last multiple-coincidence information and the last-but-one multiple-coincidence information, and further for communicating a detection result to the next multiple-coincidence counting means and the next-but-one multiple-coincidence counting means.

26. The ATM header conversion circuit according to claim 10, further comprising:

first multiple-coincidence counting means placed in an odd-number position for counting the coincidences with a plurality of entry data on the basis of a collation result on each entry data stored in said entry data storage means and the last multiple-coincidence information on said entry data and further for communicating a count result to the next multiple-coincidence counting means; and

second multiple-coincidence counting means placed in an even-number position for detecting the coincidences with a plurality of entry data on the basis of a collation result on each entry data stored in said entry data storage means, the last multiple-coincidence information and the last-but-one multiple-coincidence information, and further for communicating a detection result to the

next multiple-coincidence counting means and the next-but-one multiple-coincidence counting means.

27. The ATM header conversion circuit according to claim 1, further comprising:

first multiple-coincidence counting means placed in other than position in multiples of a natural number N for detecting the coincidences with a plurality of entry data on the basis of a collation result on each entry data stored in said entry data storage means and the last multiple-coincidence information on said entry data and further for communicating a detection result to the next multiple-coincidence counting means; and

second multiple-coincidence counting means placed in a multiple-of-N position for detecting the coincidences with a plurality of entry data on the basis of a collation result on each entry data stored in said entry data storage means, the last multiple-coincidence information and the last-but-N-1 multiple-coincidence information, and further for communicating a detection result to the next multiple-coincidence counting means and the next-but-N-1 multiple-coincidence counting means.

28. The ATM header conversion circuit according to claim 10, further comprising:

first multiple-coincidence counting means placed in other than position in multiples of a natural number N for detecting the coincidences with a plurality of entry data on the basis of a collation result on each entry data stored in said entry data storage means and the last multiple-coincidence information on said entry data

and further for communicating a detection result to the next multiple-coincidence counting means; and

second multiple-coincidence counting means placed in a multiple-of-N position for detecting the coincidences with a plurality of entry data on the basis of a collation result on each entry data stored in said entry data storage means, the last multiple-coincidence information and the last-but-N-1 multiple-coincidence information, and further for communicating a detection result to the next multiple-coincidence counting means and the next-but-N-1 multiple-coincidence counting means.

29. The ATM header conversion circuit according to claim 1, further comprising:

first multiple-coincidence counting means placed in other than position in the Mth power of 2 (M represents a natural number) for detecting the coincidences with a plurality of entry data on the basis of a collation result on each entry data stored in said entry data storage means and the last multiple-coincidence information on said entry data and further for communicating a detection result to the next multiple-coincidence counting means; and

second multiple-coincidence counting means placed in a position in the Mth power of 2 for detecting the coincidences with a plurality of entry data on the basis of a collation result on each entry data stored in said entry data storage means, the last multiple-coincidence information and the last-but-2^T-1 (T represents all natural numbers below M) multiple-coincidence information, and further for communicating a detection result to the next multiple-coincidence counting means and the next-but-2^T-1 multiple-coincidence counting means.

30. The ATM header conversion circuit according to claim 10, further comprising:

first multiple-coincidence counting means placed in other than position in the Mth power of 2 (M represents a natural number) for detecting the coincidences with a plurality of entry data on the basis of a collation result on each entry data stored in said entry data storage means and the last multiple-coincidence information on said entry data and further for communicating a detection result to the next multiple-coincidence counting means; and

second multiple-coincidence counting means placed in a position in the Mth power of 2 for detecting the coincidences with a plurality of entry data on the basis of a collation result on each entry data stored in said entry data storage means, the last multiple-coincidence information and the last-but-2^T-1 (T represents all natural numbers below M) multiple-coincidence information, and further for communicating a detection result to the next multiple-coincidence counting means and the next-but-2^T-1 multiple-coincidence counting means.

31. The ATM header conversion circuit according to claim 1, further comprising:

first multiple-coincidence counting means placed in other than position in the Mth power of N (M, N represent a natural number) for detecting the coincidences with a plurality of entry data on the basis of a collation result on each entry data stored in said entry data storage means and the last multiple-coincidence information on said entry data and further for communicating a

detection result to the next multiple-coincidence counting means; and

second multiple-coincidence counting means placed in a position in the Mth power of N for detecting the coincidences with a plurality of entry data on the basis of a collation result on each entry data stored in the entry data storage means, the last multiple-coincidence information and the last-but-N^T-1 (T represents all natural numbers below M) multiple-coincidence information, and further for communicating a detection result to the next multiple-coincidence counting means and the next-but-N^T-1 multiple-coincidence counting means.

32. The ATM header conversion circuit according to claim 10, further comprising:

first multiple-coincidence counting means placed in other than position in the Mth power of N (M, N represent a natural number) for detecting the coincidences with a plurality of entry data on the basis of a collation result on each entry data stored in said entry data storage means and the last multiple-coincidence information on said entry data and further for communicating a detection result to the next multiple-coincidence counting means; and

second multiple-coincidence counting means placed in a position in the Mth power of N for detecting the coincidences with a plurality of entry data on the basis of a collation result on each entry data stored in the entry data storage means, the last multiple-coincidence information and the last-but-N^T-1 (T represents all natural numbers below M) multiple-coincidence information, and further for communicating a detection result to the next multiple-

coincidence counting means and the next-but-N^T-1 multiple-coincidence counting means.

33. An ATM header conversion method for an optical subscriber transmission system, comprising the steps of:

storing, as entry data, first and second ATM header data paired at each of a plurality of addresses;

partially collating inputted header data with one of said first and second ATM header data stored by said storing step for each address on the basis of a designation signal representative of a collation position of said ATM header data being converted;

outputting a collation result for each address;

extracting, on the basis of the collation result for each address, an address, stored by said storing step, at which the collation result shows coincidence; and

outputting, as converted ATM header data, the other of said first and second ATM header data at said address extracted by said extracting step.

34. An ATM header conversion method for an optical subscriber transmission system, comprising the steps of :

storing ATM header data, which remain unchanged before and after conversion, as entry data in a state associated with first and second addresses paired;

fully collating inputted header data with said ATM header data, stored by said storing step, at each of said pairs of first and second addresses to output a collation result at each of said pairs of first and second addresses;

extracting, on the basis of said collation result at each of said pairs of first and second addresses, said first and second addresses storied by said storing step at which said collation result shows coincidence;

storing in advance, in a converted ATM header storage means, said ATM header data after conversion in a state associated with said first and second addresses stored by said storing step; and

selecting one of said first and second addresses extracted by said extracting step on the basis of a direction of the ATM header conversion to read out said ATM header data at the selected address from said converted ATM header storage means.

35. An ATM header conversion method, comprising the steps of:

storing first and second ATM header data in a state paired with respect to each of a plurality of addresses;

collating inputted header data with one of the stored first and second ATM header data at each address on the basis of a collation position of said ATM header data being converted

selecting the other of said first and second ATM header data at an address where a collation result shows coincidence as converted ATM header data.